As an electrical engineer for IBM, my responsibilities require me to monitor SRAM chip yield and inspect bit-fail-maps for any fail patterns driven by electrical defects. Recently, SRAM yield was impacted by a swath of failing chips that extend from the left to the right of the wafer, like a ribbon. What is interesting about this signature is that the position of the swath varies wafer to wafer. By matching the yield of each wafer with the positioning of the swaths, I discovered that the worst yielding wafers have the ribbon of fails across the middle of the wafer while the better yielding wafers have the ribbon across the bottom of the wafer. I hypothesized that the “shifting” of the swaths will show some kind of order correlation and pinpoint which process is causing the defects. With that in mind, I pulled the slot order for each of the process steps. I then chose a couple of the lowest yielding wafers because I believed that if a slot order correlation exists, these wafers would be processed first, or last. I ran two different filters and came up with a small list of process steps where the worst wafers were processed first, and then each subsequent wafer had a slight improvement of yield. By consulting design engineers, I then isolated the most probable process steps from the list of possible culprits. As more and more lots came through with the same defect signature, I analyzed them based on my list of likely process steps and concluded that they all spend over 7 hours in the Siconi etch tool. The cause of these defects has not yet been verified, but by keeping the process step under 7 hours, this signature has yet to resurface, and the SRAM yield was subsequently improved.